

CSCE 4610/5610: Computer Systems Architecture

You May Want To Know

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(Other times by appointment only)

Tentative Breakdown Of Course Grades

	CSCE 4610	CSCE 5610
Quizzes	40%	40%
Final	20%	20%
Homework Assignments (including programming projects)	35%	25%
Term Project		10%
Discretion	5%	5%

The purpose of this course is to provide you with a solid foundation in computer systems architecture. This course is generally considered as a foundation to further study and research in computer systems. We will survey several different approaches to designing a single CPU that can aid in building a parallel processor. We will investigate instruction level parallelism, branch prediction techniques, various cache organization, multithreaded architectures, cache coherency and their impact on parallel processing.

Prerequisites: Computer Organization (CSCE 2610 or CSCI 3100) and Systems Programming (CSCIE3600). Primarily, I would like to see that you know how a basic CPU works (including instruction fetch, decode, execute cycles, microprogramming), instruction sets and choices (including RISC versus CISC, address modes), memory organization (including virtual memory, memory interleaving), some I/O (including interrupts, polling, daisy chaining, serial and parallel I/O), ALU (including multiplication, division and floating point algorithms), synchronization and mutual exclusion (like semaphores), some understanding of networks and protocols, some understanding of compilers and runtime support, Operating system concepts like process scheduling, virtual memory, protection domains, etc.

If you need a refresher, take a look at, "Computer Organization and Design" by Hennessy and Patterson.

Exams and Grading Policies: All my exams (mid-semester and final) are "open-book" format. The final exam is not comprehensive. I grade every exam using a "relative point" system. For each problem, I select the best among all the solutions presented by the students (which gets the highest grade) and grade all the others relative to the best solution.

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Course Outline

	Hours
1. Introduction and Background	6
What is computer architecture	
Instruction sets, control unit	
Performance evaluation	
2. Pipelining	10
Basic design of pipelines	
Data and control hazards	
Branch prediction and dynamic scheduling	
Superscalar and multiple issue processors	
VLIW or EPIC	
3. Dataflow and multithreaded architectures	6
Dataflow model of computation	
What is multithreading	
Scheduled Dataflow	
SMT and Hyper Threading	
4 Cache Memories	8
Cache memory designs	
Improving cache performance	
Cache coherency	
5. Shared Memory Multiprocessors	6
Mutual Exclusion and Synchronization	
Cache Coherency Problem and Solutions	
Distributed Shared Memory Systems	
6. Low Power Issues	4

Textbook: J. Hennessy and D. Patterson. "Computer Architecture: A Quantitative Approach", 3rd Edition (or 4th edition)

Other Useful Books:

1. J.P. Shen and M.H. Lipasti. "Modern Processor Design", McGraw Hill, 2005
2. D.E. Culler and J.P. Singh. "Parallel Computer Architecture", Morgan Kaufman, 1999